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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/779,424	02/08/2001	Paras A. Shah	COMP:0187/FLE (P00-3008)	5601

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INTELLECTUAL PROPERTY ADMINISTRATION
LEGAL DEPARTMENT, M/S 35
P.O. BOX 272400
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EXAMINER	
KNOLL, CLIFFORD H	
ART UNIT	**PAPER NUMBER**
2112	

DATE MAILED: 03/28/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/779,424	SHAH, PARAS A.	
	Examiner	Art Unit	
	Clifford H Knoll	2112	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-19,21,22,24-26,28,29* is/are rejected.

7)☒ Claim(s) *20,23,27 and 30* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *08 February 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This Office Action is responsive to communication filed 1/24/05. Currently claims 1-30 are pending.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

1. *Claims 1-15 are rejected under 35 U.S.C. 102(e) as being anticipated by MacLaren (US 6108741).*

> The applied reference has a common assignee with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 102(e) might be overcome either by a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not the invention "by another," or by an appropriate showing under 37 CFR 1.131.

Regarding claims 1, 6, 9, and 12, discloses temporarily storing a plurality of transaction entries (e.g., col. 28, lines 34-37), selecting one of the plurality of temporarily stored transaction entries and enqueuing the selected one of the plurality of temporarily stored transaction entries (e.g., col. 29, lines 64-66).

Regarding claims 2, 7, 10, and 13, MacLaren also discloses wherein (a) temporarily stores a plurality of transaction entries in a bank of registers (e.g., col. 28, lines 34-37).

Regarding claim 3, MacLaren also discloses wherein the plurality of transaction entries is temporarily stored simultaneously (e.g., col. 14, lines 22-23).

Regarding claims 4, 8, 11, and 14 MacLaren also discloses determining whether a posted write transaction entry is present; if the posted write transaction entry is present, then enqueuing the posted write transaction entry into the transaction order queue (e.g., col. 26, lines 60-63), if the posted write transaction entry is not present, then determining whether a read completion transaction entry is present; if the read completion transaction entry is present, then enqueuing the read completion transaction entry into the transaction order queue (e.g., col. 29, lines 17-26, though not represented in MacLaren's "TRQ" they are nonetheless enqueued as claimed); if the read completion transaction entry is not present, then determining whether a delayed/split transaction entry is present; and if the delayed/split transaction entry is present, then enqueuing delayed/split transaction entry into the transaction order queue (e.g., col. 29, lines 13-15).

Regarding claims 5 and 15, MacLaren also discloses enqueuing each of the plurality of transaction entries into the transaction order queue one at a time during successive clock cycles (e.g., col. 30, lines 30-37).

2. *Claims 16-19, 21-22, 24-26, and 28-29 are rejected under 35 U.S.C. 102(e) as being anticipated by Olarig (US 6175889).*

> The applied reference has a common assignee with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 102(e) might be overcome either by a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not the invention "by another," or by an appropriate showing under 37 CFR 1.131.

Regarding claim 16, Olarig discloses logic and registers configured to receive transaction entries (e.g., col. 17, lines 55-58), second logic device adapted to receive the transaction entries according to PCI-X specifications (e.g., col. 11, lines 8-24), a transaction order queue configured to receive and enqueue the selected transaction entries (e.g., col. 17, line 67 – col. 18, line 3, "420").

Regarding claim 17, Olarig also discloses the input source (e.g., col. 11, lines 8-24).

Regarding claim 18, Olarig also discloses storing the plurality of transaction entries (e.g., col. 17, lines 55-58).

Regarding claim 19, Olarig also discloses selecting a single entry (e.g., col. 17, line 67 – col. 18, line 3, "420").

Regarding claim 21, Olarig also discloses enqueuing one transaction entry per clock cycle (e.g., col. 17, lines 60-64, "430", "433").

Regarding claim 22, Olarig discloses one processor and a memory device operatively coupled to the at least one processor; and a transaction order queue circuit configured to process transactions from the memory device (e.g., col. 11, lines 50-51),

the transaction order queue circuit being adapted to encode a plurality of simultaneously received transaction entries (e.g., col. 17, lines 55-58).

Regarding claim 24, Olarig also discloses wherein the computer system comprises network capabilities (e.g., col. 14, lines 3-5).

Regarding claim 25, Olarig discloses temporarily storing a plurality of simultaneous transaction entries (e.g., col. 17, lines 55-58); and delivering the plurality of transaction entries to a transaction order queue one at a time (e.g., col. 17, line 67 – col. 18, line 3, "420").

Regarding claim 26, Olarig also discloses the plurality of simultaneous transaction entries is stored in a bank of registers (e.g., col. 17, lines 55-58).

Regarding claim 28, Olarig discloses temporarily storing a plurality of simultaneous transaction entries (e.g., col. 17, lines 55-58); and delivering the plurality of transaction entries to a transaction order queue one at a time (e.g., col. 17, line 67 – col. 18, line 3, "420").

Regarding claim 29, Olarig also discloses the plurality of simultaneous transaction entries is stored in a bank of registers (e.g., col. 17, lines 55-58).

Allowable Subject Matter

3. *Claims 20, 23, 27, and 30 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.*

Response to Arguments

Applicant's arguments filed 1/24/05, with respect to claims 1, 6, 9, and 12, have been fully considered but they are not persuasive.

Applicant's arguments with respect to claims 16-19, 21-22, 25, and 28 have been considered but are moot in view of the new ground(s) of rejection.

Regarding claim 1, Applicant argues that MacLaren does not disclose "prioritizing transaction entries according to a bus standard"; however, MacLaren, as cited supra, does prioritize according to a bus standard. As noted by MacLaren, "[a]ccording to the PCI Spec 2.1, PCI-to-PCI bridges must strongly favor posted write transactions when determining the order in which transactions are to be performed on the target bus. The PCI Spec 2.1 requires that, in order to prevent lock-up conditions, the computer system must allow posted write cycles to bypass earlier-initiated delayed request cycles and must prevent delayed request cycles from bypassing earlier-initiated posted write cycles" (col. 1, lines 19-36), which establishes the bus standard desideratum in prioritization. Now the question remains as to whether the claimed "each of the plurality of temporarily stored transaction entries are prioritized" is disclosed. MacLaren discloses "[t]ransactions in the TOQ 2272 must remain in the TOQ 2272 until the posted memory write transaction is removed from the TRQ 2270 (col. 28, lines 42-44). The Examiner finds that this feature anticipates prioritization of entries as claimed.

Applicant further argues that "TOQ 2272 is a first-in-first out (FIFO) queue"; however, this feature does not prevent the interpretation of the TOQ used supra. In

MacLaren, Examiner agrees that entries are output from the TOQ in order; however, output from the TOQ is prevented altogether in the instance noted supra and this feature of the TOQ is relied upon as a prioritization, and in particular as a prioritization that is performed according to a bus standard.

Applicant notes that "transactions in the TRQ 2270 are completed 'in the order they were received' Col. 26, lines 63-65" (p. 14); however, this passage refers to the TOQ, not the TRQ. In fact, in the TRQ, the "circular output pointer 2294 arbitrates between the transactions in the TRQ 2270 and determines their order of execution" (col. 27, lines 35-37).

Regarding claim 12, Applicant argues that in MacLaren "[t]here is no act of 'ordering...according to a bus standard' in the TOQ or the TRQ. The TOQ and the TRQ are simply enqueued as they are received"; however, as treated supra, this is incorrect, as an order of execution" (col. 27, lines 35-37) is determined for the TRQ. Thus, the Examiner finds the TRQ as anticipatory of "logic adapted for selecting and ordering..." while the TOQ is anticipatory of the claimed "temporary memory storage".

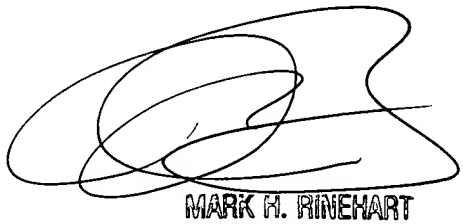
Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Clifford H Knoll whose telephone number is 571-272-3636. The examiner can normally be reached on M-F 0630-1500.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark H Rinehart can be reached on 571-272-3632. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

chk



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